



High speed data processing engine

EXpresso G2



EXpresso series products

EXpresso G4
EXpresso FPGA

EXpresso G2
EXpresso

OUTLINE

This board is a high speed hardware accelerator for image data processing and NGN (Next Generation Network) with a state-of art FPGA chip. It is possible that many kinds of algorithm for 3D big image data processing, semi-conductor inspection, medical image processing, signal processing application and so on are implemented in the FPGA.

SPECIFICATION

FPGA

Stratix II GX EP2SGX130

Memory configuration

- DDDR2 SDRAM memory 2G bytes SO-DIMM 1 bank
- QDRII SRAM memory 18M bytes 2 banks

Interface

Host PC interface

PCI Express x8

CameraLink interface card (OPTION)

Base/Medium/Full configuration: 1 channel

Base configuration: 2 channels Base configuration: 4 channels

[Interface specification]

- Many kinds of trigger signal input for example: A-Phase, B-Phase and Z-Phase
- Encoder logic, timer logic
- 4-bit input, 2-bit output PIO (200KHz)
- Isolation by photo-coupler
- HD-SDI interface card (OPTION)

HD-SDI hi-vision image input x 2

HD-SDI loop-back output x 2



CameraLink (OPTION)
* daughter card



HD-SDI (OPTION)
*daughter card



Soliton Systems K.K. Shinjuku 2-4-3, Shinjuku-ku, Tokyo 160-0022, JAPAN www.soliton.co.jp Development & Sales: Embedded System Div. TEL +81-3-5360-3851 FAX +81-3-5360-3888 eMail: at@soliton.co.jp